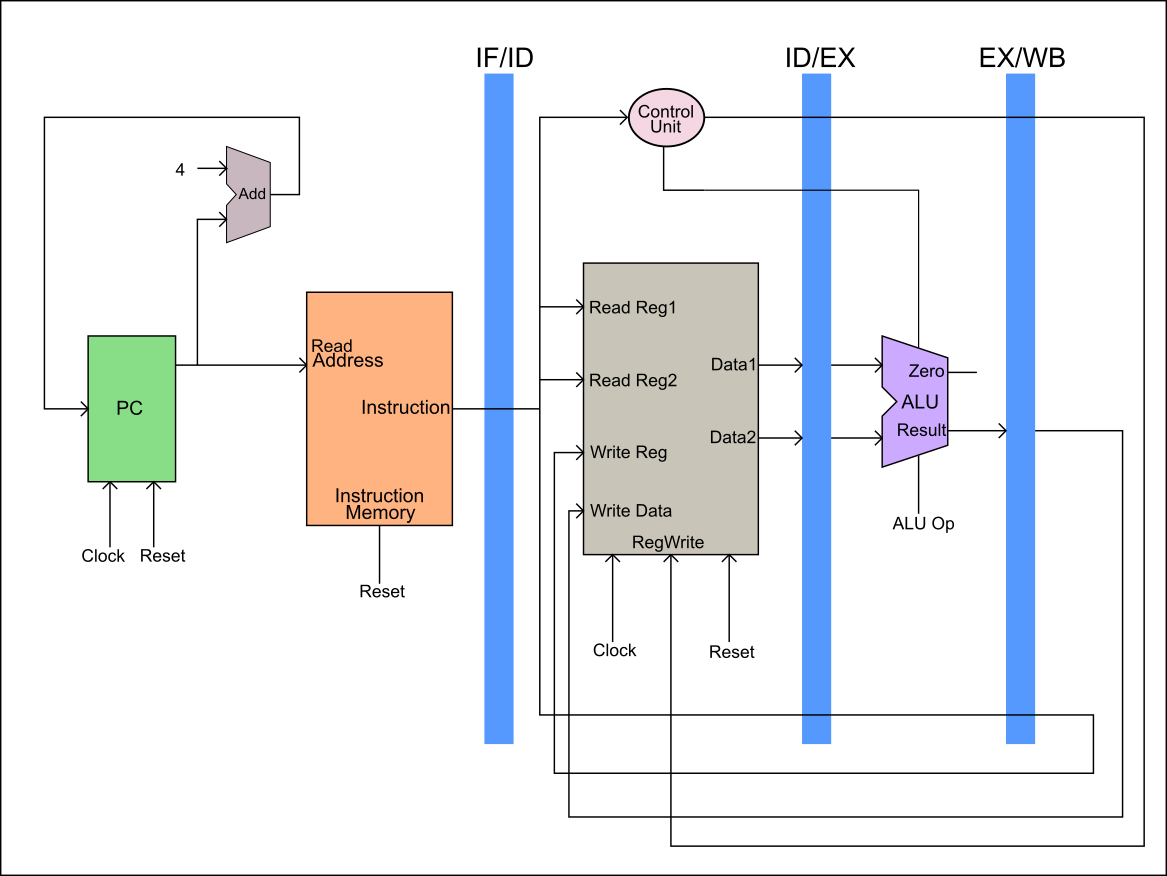
**Experiment No 8: Implementation of a Pipelined Processor for R-type Instructions**

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| --- | --- | --- |
| **Sl No** | **Name** | **ID No** |
| **1** | **VISHWAS VASUKI GAUTAM** | **2019A3PS0443H** |

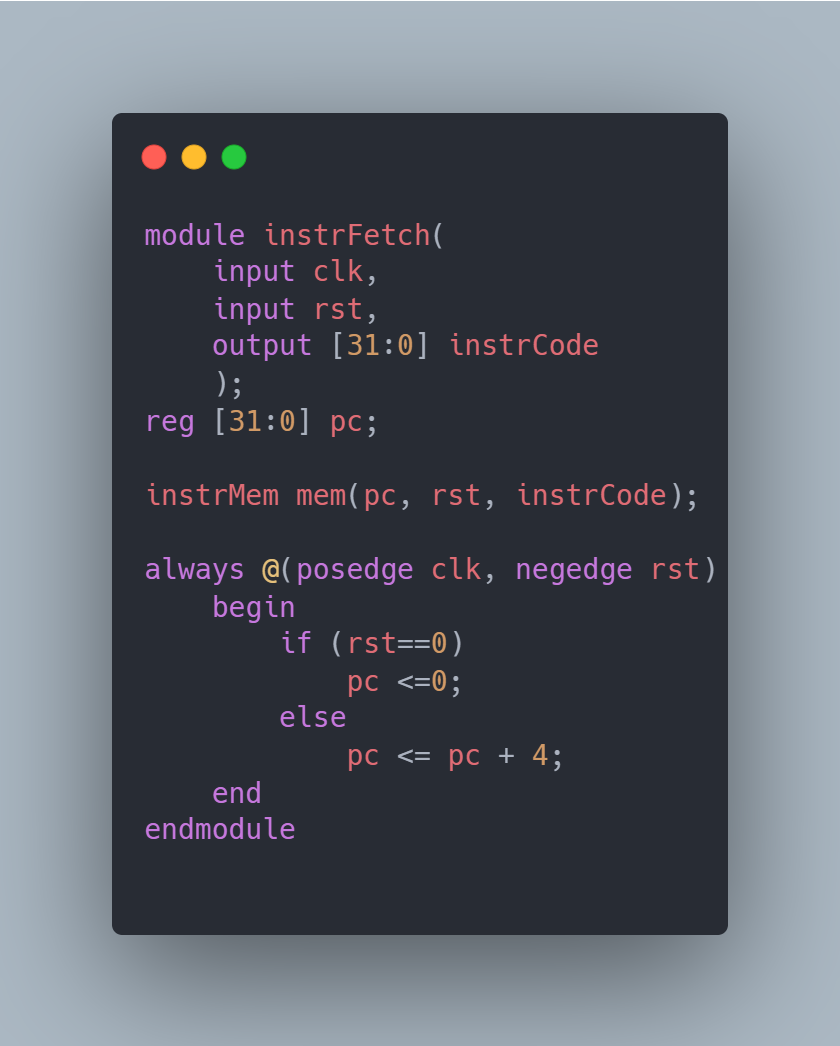
# Implement partial RISC V pipelined processor (Shown below), which executes only R-Type instructions. (Make use of the blocks implemented earlier)

This processor should support the following instructions (Please refer RISC V reference manual for the opcodes, func7 and func3 codes for instructions. Accordingly generate the correct ALU operation bits):

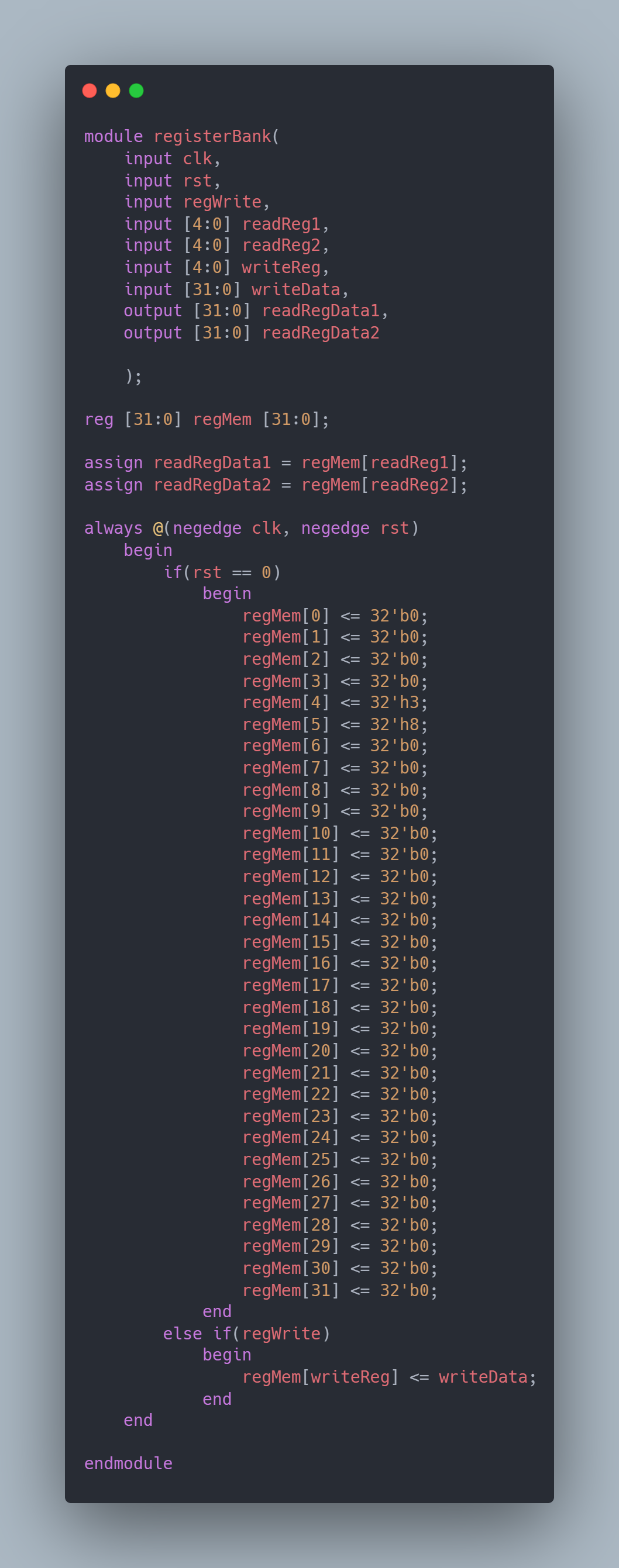
|  |
| --- |
| **add** |
| **sub** |
| **AND** |
| **OR** |
| **sll** |
| **srl** |



1. **Implement the Instruction Fetch block. Copy the image of Verilog code of the Instruction fetch block here**

Answer: 

1. **Implement the Register File and copy the image of Verilog code of Register file unit here.**

Answer: ****

1. **Implement the main control unit and copy the image of Verilog code of Main control unit here.**

Answer: 

1. **Implement complete pipelined processor in Verilog (Instantiate all the datapath blocks and main control unit as modules). Copy the image of Verilog code of the processor here.**

Answer: ****

1. **Test the processor design by initializing the instruction memory with a set of instructions. List below the sequence of instructions you have used to initialize the instruction memory. Verify if the register file is changing according to the instructions. (Register file contains unknowns, you can initialize the register file or you can load values into the register file using li instruction specified earlier).**

Sequence of Instructions Implemented:   
add t2, t0, t1   
sub s0, t0, t1 |  
and s1, t0, t1

1. **Verify if the register file is getting updated according to your sequence of instructions (mentioned earlier).**

Copy verified **Register file** waveform here (show only the Registers that get updated, CLK, and RESET):   
  


1. **List the concepts you learnt from this experiment (Conclusions/Observations)**

Answer: **In this lab we learnt to modify the files and make a pipelined processor.**